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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,952	08/29/2001	William R. Wheeler	10559-597001	6372

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EXAMINER	
SHAAWAT, MUSSA	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,952	WHEELER ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☒ Claim(s) [redacted] is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/11/03,12/29/03,* 3/15/04 M.S.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to Application # 09/941,952, filed on August 29, 2001. Claims 1-30 are presented for examination.

Claim Interpretation

2. Claims 4, 14, and 24, recite, "Code comprises one of c++ and Verilog". The examiner interprets, "code comprises one of C++ and Verilog" to mean, "code comprises one of C++ or Verilog".

Specification

3. The Abstract is objected to because it contains legal phraseology. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-10 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.

Specifically, claim 1 is not technologically embodied and merely recite "representing the combinatorial logic and state logic using graphical elements" that could be carried out by a combination of paper and pencil calculations.

Claims 2-10 depend from claim 1; therefore they inherit the same deficiencies.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-3, 7, 9-10, 11-13, 17, 19-20, 21-23, 27, and 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Daniel Watkins US Patent No. (5,220,512) referred to hereinafter as Watkins.

As per claim 1, Watkins teaches a method of simulating a logic design comprised of combinatorial logic (see Fig.3 block 308 shows gates which are combinatorial logic elements) and state logic (see Fig.3 block 302 shows a flip-flop

which is a state logic element), the method comprising: representing the combinatorial logic and the state logic using separate graphic elements (see col.5 lines 35-44, Fig.3, where objects "gates and flip-flops" represent circuit compnents); and

Associating computer code that simulates portions of the logic design with a graphic element that represents the combinatorial logic and with a graphic element that represents the state logic (see col. 5 lines 45-52, col.5 lines 62-68, and Fig.3, where the graphical symbols of the circuit "gates and flip-flops" are connected or associated via program code).

As per claim 2, Watkins teaches a method of claim 1, further comprising: performing an error check on the graphic elements to determine if a single graphic element represents both combinatorial logic and state logic (see col.6 lines 3-4, Fig.3, where the logic verifier checks the schematics for design errors of multiple outputs connected together of "graphical elements which include combinational logic and state logic"); and

Issuing an error message if the single graphic element represents both combinatorial logic and state logic (see col.5 lines 5-6, where generating an error indication of any problems that exist which design corresponds to issuing an error message).

As per claim 3, Watkins teaches a method of claim 1, further comprising: generating intermediate code that simulates the logic design (see col.9 lines 64-65, where the logic compiler creates a schematic object file or files corresponds to generating intermediate code); and

Generating the computer code from the intermediate code (see claim.8, where executable simulation corresponds computer code).

As per claim 7, Watkins teaches a method of claim 1, further comprising: generating a topology of the logic design based on the graphic elements (see Fig.3, shows a diagram of graphical elements of the logical design of gates and flip-flops); obtaining clock domains from the topology; and generating the computer code based on the clock domains (see col.9 lines 55-59, where macros are code of graphical elements programmed to move through an interactive simulation in cycle clock domains).

As per claim 9, Watkins teaches a method of claim 1, wherein state elements comprise elements, which hold a particular logic state for a period of time (see Fig.3 block 302 shows a flip-flop which is a state logic element) and combinatorial logic elements comprise elements which combine two or more states to produce an output (see Fig.3 block 308 shows gates which are combinatorial logic elements).

As per claim 10, Watkins teaches a method of claim 1, wherein the graphic elements comprise block diagrams (see Fig.3 shows a block diagram of the logic state and combinational state diagrams).

As per claims 11-13, the limitations of claims 11-13 are similar to the limitations of claims 1-3; therefore they are rejected based on the same rationale, supra.

As per claim 17, the limitations of claims 17 are similar to the limitations of claim 7; therefore it is rejected based on the same rationale, supra.

As per claims 19-20, the limitations of claims 19-20 are similar to the limitations of claims 9-10; therefore they are rejected based on the same rationale, supra.

As per claims 21-23, the limitations of claims 21-23 are similar to the limitations of claims 1-3; therefore they are rejected based on the same rationale, supra.

As per claim 27, the limitations of claims 27 are similar to the limitations of claim 7; therefore it is rejected based on the same rationale, supra.

As per claims 29-30, the limitations of claims 29-30 are similar to the limitations of claims 9-10; therefore they are rejected based on the same rationale, supra.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6, 14-16, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claim 1 above in view of Michael Reynolds US Patent No. (6,480,985) referred to hereinafter as Reynolds.

As per claim 4, although Watkins teaches a user interacts with the ECAD system's through the use of an object-oriented user interface, which can include C++ code (see col.5 lines 35-36), he does not expressly teach a computer code comprising C++.

Reynolds teaches the use of C++ code for graphically representing an IC design circuit (see col.8 lines 48-49)

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teachings of Reynolds and Watkins because C++ would enable users of Watkins' system to more conveniently generate graphical representation of integrated circuits from remote workstations.

As per claim 5, Watkins teaches a method of claim 4, wherein, if the computer code comprises C++, the method further comprises running the code through a cycle-based simulator to provide a simulation of the operation of the logic design (see col.11 lines 16-17, Fig.3, where one stepped simulation cycle of timing program corresponds to running the code through a cycle base simulator).

As per claim 6, Watkins teaches running the code through an event-driven simulator to provide a simulation of the operation of the logic design (see col.11 lines 15-16, where the graphical depiction of the state events that occurred during simulation of the timing program corresponds to running a code through an event-driven simulator). However Reynolds does not teach the use of a verilog code.

Reynolds teaches the use of verilog code (see col.2 lines 43-45)

It would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to combine the teachings of Reynolds and Watkins because Verilog is a widely used hardware description language and would enable the system to be more compatible.

As per claims 14-16, the limitations of claims 14-16 are similar to the limitations of claims 4-6; therefore they are rejected based on the same rationale, supra.

As per claims 24-26, the limitations of claims 24-26 are similar to the limitations of claims 4-6; therefore they are rejected based on the same rationale, supra.

6. Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins as applied to claim 7 above in view of Michael Rostoker US Patent No. (5,544,067) referred to hereinafter as Rostoker.

Watkins discloses all the claimed limitations as applied in claim 7 above.

As per claim 8, Watkins does not expressly teach dividing the computer program into segments and compiling the segments separately.

However Rostoker in a similar configuration and analogous art discloses in col. 5 lines 64-67, that " in order to simulate a small portions of a circuit (segment), the user may need to design special test circuits incorporating those small test circuits of the circuit and simulate them in isolation" (emphasis added). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Rostoker's limitations of simulating small portions of a circuit i.e., dividing a program into segments with Watkins because it will enable a user to test portions of a circuit (segment) in isolation.

As per claim 18, the limitations of claims 18 are similar to the limitations of claim 8. Therefore it is rejected based on the same rationale, supra.

As per claim 28, the limitations of claims 28 are similar to the limitations of claim 8. Therefore it is rejected based on the same rationale, supra.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ashar et al. US Patent No. (6,745,160) Verification of scheduling in the presence of loops using uninterrupted symbolic simulation.
- Lin et al. US Patent No. (6,389,379) Coverification system and method.
- Okumura US Patent No. (6,560,947) Logic simulation method and logic simulator.
- Tochio et al US Patent No. (5,911,061) Program Data creating method and apparatus for use with programmable device in s logic emulation system.
- Stewart et al US Patent No. (6,223,148) Logic analysis system for logic emulation systems.

Communication

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571) 272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
January 13, 2005

JEAN R. HOMERE
PRIMARY EXAMINER